

**What Is Claimed Is:**

1        1. A method of converting an analog signal to accurate output digital codes of N-bits  
2        each, said method being performed in an analog to digital converter (ADC), said method  
3        comprising:  
4              receiving said analog signal;  
5              converting a sample of said analog signal into a N-bit digital code;  
6              generating a difference voltage of said sample and a voltage level represented by said  
7        N-bit digital code;  
8              converting said difference voltage into a P-bit digital code, wherein P is less than N;  
9        and  
10         determining an accurate output digital code from said N-bit digital code and said P-bit  
11        digital code.

1        2. The method of claim 1, further comprising:  
2              generating said difference voltage at a plurality of time points;  
3              performing said converting said difference voltage a corresponding number of times  
4        to generate a corresponding plurality of P-bit digital codes;  
5              determining an average of said plurality of P-bit digital codes; and  
6              performing an addition operation based on said average and said N-bit digital code  
7        to generate said accurate output digital code.

1        3. The method of claim 2, wherein said difference voltage changes due to internal  
2        noise in said ADC and said addition operation reduces the effect of said internal noise in the

3 value generated for said accurate output digital code.

1       4. The method of claim 3, wherein said P is substantially smaller than said N, and  
2 equals an integer not less than  $[\log_2 (6 * \sigma_{tot})]$ , wherein \* represents a multiplication  
3 operation, and  $\sigma_{tot}$  represents a total of said internal noise.

1       5. The method of claim 2, wherein said addition operation corrects said N-bit digital  
2 code in either positive direction or negative direction according to said P-bit digital code.

1       6. The method of claim 5, wherein said ADC comprises N first set of capacitors and  
2 P second set of capacitors, wherein said first set of capacitors are operated according to  
3 successive approximation principle (SAP) to determine said N bit digital code, and said  
4 second set of capacitors are thereafter operated according to said SAP to determine said P-bit  
5 digital code, said method further comprising:

6           sampling said sample on said first set of capacitors in a sampling phase, wherein said  
7 sampling is performed before converting said sample into said N-bit digital code;

8           connecting a first capacitor contained in said second set of capacitors to a Vref voltage  
9 and the remaining ones of said second set of capacitors to ground in said sampling phase,  
10 wherein said first capacitor corresponds to a most significant bit (MSB) of said P-bit digital  
11 code;

12           adding all but the MSB of said P-bit digital code to said N-bit digital code if the MSB  
13 of said P-bit digital code is of one logical value; and

14           subtracting all but the MSB of said P-bit digital code from said N-bit digital code if

15 the MSB of said P-bit digital code is of the other logical value.

1           7. A successive approximation type analog to digital converter (SAR ADC)  
2 converting a sample of an input analog signal into an accurate N-bit digital code, said SAR  
3 ADC comprising:

4           a comparator providing a comparison result of a first analog signal and said sample;  
5           a digital to analog converter (DAC) receiving an intermediate N-bit value and an  
6 intermediate P-bit value, said DAC generating said first analog signal based on said  
7 intermediate N-bit value and said intermediate P-bit value; and

8           a SAR logic determining a first N-bit digital code according to successive  
9 approximation principle (SAP) by sending said intermediate N-bit value in each of N  
10 iterations, said SAR logic then generating a first P-bit digital code according to said SAP by  
11 sending said intermediate P-bit value in each of P iterations, wherein said first N-bit digital  
12 code is corrected using said first P-bit digital code to generate said accurate N-bit digital  
13 code.

1           8. The SAR ADC of claim 7, wherein said SAR logic determines a plurality of P-bit  
2 digital codes including said first P-bit digital code, said plurality of P-bit digital codes being  
3 averaged to generate an average value, wherein said first N-bit digital code is corrected using  
4 said average value.

1           9. The SAR ADC of claim 8, wherein said DAC comprises:

2           N first set of capacitors, each having a capacitance value corresponding to a weight

3 of a corresponding one of a N-bit code;

4           N first set of switches, wherein each of said first set of switches connects a  
5 corresponding one of said first set of capacitors to said sample in a sampling phase of said  
6 SAP, each of said first set of switches connecting a corresponding one of said first set of  
7 capacitors to a ground or a reference voltage according to a corresponding bit of said  
8 intermediate N-bit value in a conversion phase of said SAP;

9           P second set of capacitors, each having a capacitance value corresponding to a weight  
10 of a corresponding one of a P-bit code, wherein P is less than N; and

11          P second set of switches, each of said second set of switches connecting a  
12 corresponding one of said second set of capacitors to a ground or a reference voltage  
13 according to a corresponding bit of said intermediate P-bit value.

1           10. The SAR ADC of claim 9, wherein another end of each of said first set of  
2 capacitors and said second set of capacitors is connected to a  $V_{mid}$  voltage by a third switch,  
3 wherein said third switch is in a closed state in said sampling phase and in an open state in  
4 said conversion phase, wherein an intermediate analog signal equaling the following voltage  
5 is generated by said DAC:

$$V_{top} = V_{mid} - V_{inp} + \sum_{i=1}^N b_i \frac{V_{ref}}{2^i} + \sum_{j=1}^P b_j \frac{V_{ref}}{2^j}$$

6           wherein  $V_{ref}$  and  $V_{inp}$  represent said reference voltage and voltage of said sample, and  
7            $b_i$  represents the  $i^{th}$  bit of said intermediate N-bit value and  $b_j$  represents the  $j^{th}$  bit of said  
8           intermediate P-bit value.

1           11. The SAR ADC of claim 10, wherein said comparator compares said intermediate

2 analog signal with said  $V_{mid}$  voltage to generate said comparison result.

1           12. The SAR ADC of claim 11, wherein said average value is used to correct said first  
2 N-bit digital code in either positive or negative direction.

1           13. The SAR ADC of claim 12, wherein SAR logic sets a most significant bit (MSB)  
2 of said P-bit digital code to one in said sampling phase, and adds all but the MSB of said  
3 average value to said N-bit digital code if the MSB of said average value is of one logical  
4 value, said SAR logic subtracting all but the MSB of said average value from said N-bit  
5 digital code if the MSB of said P-bit digital code is of the other logical value.

1           14. The SAR ADC of claim 13, wherein said DAC comprises more than P of said  
2 second set of switches, and wherein P is determined by a noise introduced internally in said  
3 SAR ADC.

1           15. The SAR ADC of claim 13, wherein said noise comprises components introduced  
2 by said DAC and said comparator.

1           16. A successive approximation type analog to digital converter (SAR ADC)  
2 converting an analog signal to accurate output digital codes of N-bits each, said SAR ADC  
3 comprising:

4           means for receiving said analog signal;

5           means for converting a sample of said analog signal into a N-bit digital code;

6           means for generating a difference voltage of said sample and a voltage level  
7           represented by said N-bit digital code;

8           means for converting said difference voltage into a P-bit digital code, wherein P is less  
9           than N; and

10          means for determining an accurate output digital code from said N-bit digital code and  
11         said P-bit digital code.

1           17. The SAR ADC of claim 16, further comprising:

2           means for generating said difference voltage at a plurality of time points, wherein said  
3           means for converting said difference voltage converts said difference voltage a corresponding  
4           number of times to generate a corresponding plurality of P-bit digital codes;

5           means for determining an average of said plurality of P-bit digital codes; and

6           means for performing an addition operation based on said average and said N-bit  
7           digital code to generate said accurate output digital code.

1           18. The SAR ADC of claim 17, wherein said difference voltage changes due to  
2           internal noise in said SAR ADC and said addition operation reduces the effect of said internal  
3           noise in the value generated for said accurate output digital code.

1           19. The SAR ADC of claim 18, wherein said P is substantially smaller than said N,  
2           and equals an integer not less than  $[\log_2(6 * \sigma_{\text{tot}})]$ , wherein \* represents a multiplication  
3           operation, and  $\sigma_{\text{tot}}$  represents a total of said internal noise.

1           20. The SAR ADC of claim 17, wherein said addition operation corrects said N-bit  
2       digital code in either positive direction or negative direction according to said P-bit digital  
3       code.

1           21. The SAR ADC of claim 20, wherein said means for converting a sample  
2       comprises N first set of capacitors and P second set of capacitors, wherein said first set of  
3       capacitors are operated according to successive approximation principle (SAP) to determine  
4       said N bit digital code, and said second set of capacitors are thereafter operated according to  
5       said SAP to determine said P-bit digital code, said SAR ADC further comprising:

6           means for sampling said sample on said first set of capacitors in a sampling phase,  
7       wherein said means for sampling is performed before converting said sample into said N-bit  
8       digital code;

9           means for connecting a first capacitor contained in said second set of capacitors to a  
10      Vref voltage and the remaining ones of said second set of capacitors to ground in said  
11      sampling phase, wherein said first capacitor corresponds to a most significant bit (MSB) of  
12      said P-bit digital code;

13          means for adding all but the MSB of said P-bit digital code to said N-bit digital code  
14      if the MSB of said P-bit digital code is of one logical value; and

15          means for subtracting all but the MSB of said P-bit digital code from said N-bit digital  
16      code if the MSB of said P-bit digital code is of the other logical value.

1           22. A system comprising:

2       an analog processor processing an analog signal to generate an analog sample;

3           a successive approximation type analog to digital converter (SAR ADC) converting  
4    said analog sample into an accurate N-bit digital code, said SAR ADC comprising:

5                a comparator providing a comparison result of a first analog signal and  
6    said sample;

7                a digital to analog converter (DAC) receiving an intermediate N-bit  
8    value and an intermediate P-bit value, said DAC generating said first analog  
9    signal based on said intermediate N-bit value and said intermediate P-bit  
10   value; and

11               a SAR logic determining a first N-bit digital code according to  
12    successive approximation principle (SAP) by sending said intermediate N-bit  
13    value in each of N iterations, said SAR logic then generating a first P-bit  
14    digital code according to said SAP by sending said intermediate P-bit value  
15    in each of P iterations, wherein said first N-bit digital code is corrected using  
16    said first P-bit digital code to generate said accurate N-bit digital code; and

17               a processing unit receiving said accurate output digital code.

1           23. The system of claim 22, wherein said SAR logic determines a plurality of P-bit  
2    digital codes including said first P-bit digital code, said plurality of P-bit digital codes being  
3    averaged to generate an average value, wherein said first N-bit digital code is corrected using  
4    said average value.

1           24. The system of claim 23, wherein said DAC comprises:

2               N first set of capacitors, each having a capacitance value corresponding to a weight

3 of a corresponding one of a N-bit code;

4       N first set of switches, wherein each of said first set of switches connects a  
5 corresponding one of said first set of capacitors to said sample in a sampling phase of said  
6 SAP, each of said first set of switches connecting a corresponding one of said first set of  
7 capacitors to a ground or a reference voltage according to a corresponding bit of said  
8 intermediate N-bit value in a conversion phase of said SAP;

9       P second set of capacitors, each having a capacitance value corresponding to a weight  
10 of a corresponding one of a P-bit code, wherein P is less than N; and

11       P second set of switches, each of said second set of switches connecting a  
12 corresponding one of said second set of capacitors to a ground or a reference voltage  
13 according to a corresponding bit of said intermediate P-bit value.

1       25. The system of claim 24, wherein another end of each of said first set of capacitors  
2 and said second set of capacitors is connected to a  $V_{mid}$  voltage by a third switch, wherein  
3 said third switch is in a closed state in said sampling phase and in an open state in said  
4 conversion phase, wherein an intermediate analog signal equaling the following voltage is  
5 generated by said DAC:

$$V_{top} = V_{mid} - V_{inp} + \sum_{i=1}^N b_i \frac{V_{ref}}{2^i} + \sum_{j=1}^P b_j \frac{V_{ref}}{2^j}$$

6  
7       wherein  $V_{ref}$  and  $V_{inp}$  represent said reference voltage and voltage of said sample, and  
8  
9        $b_i$  represents the  $i^{th}$  bit of said intermediate N-bit value and  $b_j$  represents the  $j^{th}$  bit of said  
10 intermediate P-bit value.

1       26. The system of claim 25, wherein said comparator compares said intermediate

2 analog signal with said  $V_{mid}$  voltage to generate said comparison result.

1           27. The system of claim 26, wherein said average value is used to correct said first N-  
2 bit digital code in either positive or negative direction.

1           28. The system of claim 27, wherein SAR logic sets a most significant bit (MSB) of  
2 said P-bit digital code to one in said sampling phase, and adds all but the MSB of said  
3 average value to said N-bit digital code if the MSB of said average value is of one logical  
4 value, said SAR logic subtracting all but the MSB of said average value from said N-bit  
5 digital code if the MSB of said P-bit digital code is of the other logical value.

1           29. The system of claim 28, wherein said DAC comprises more than P of said second  
2 set of switches, and wherein P is determined by a noise introduced internally in said SAR  
3 ADC.

1           30. The system of claim 28, wherein said noise comprises components introduced by  
2 said DAC and said comparator.

1           31. The system of claim 30, wherein said system comprises a global positioning  
2 system receiver, said system further comprising an antenna to receive said analog signal and  
3 provide to said analog processor.